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10/804,010	03/19/2004	Scott E. Harrow	10205.030DIV	6995

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EXAMINER	
SINGH, RAMNANDAN P	

ART UNIT	PAPER NUMBER
2646	

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/804,010	HARROW ET AL.	
	Examiner	Art Unit	
	Ramnandan Singh	2646	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed Nov. 14, 2005 have been fully considered but they are not persuasive.

(i) Applicant's argument---"Examiner asserts that logic for preventing roll-over is not shown because it is well-known. Is this Official Notice ? If so, it is improperly taken. Perhaps the logic is not shown because it is not there. The innards of accumulator 20 are not disclosed. Presuming a particular circuit configuration is unjustified" on pages 2-3.

Examiner's response---Examiner respectfully disagrees. In response to the above, the following details are provided:

(a) Applicant---"Examiner asserts that logic for preventing roll-over is not shown because it is well-known".

Examiner—This is not the Examiner's assertion. Viot et al assert: "The logic necessary to provide these functions (roll-over and overflow) is not shown, but is well-known" [col. 6, lines 32-33; col. 6, lines 11-32].

(b) Applicant—" Perhaps the logic is not shown because it is not there. The innards of accumulator 20 are not disclosed. Presuming a particular circuit configuration is unjustified".

Examiner—In response, Applicant is directed to Fig. 6 of Viot et al for details which shows a structure of a multi-bit pulse accumulator (20) [Fig. 6; col. 3, line 66 to col. 4, line 48; col. 4, lines 33-48; col. 11, lines 21-45]. Further, the Examiner

asserts that a counter is inherent in an accumulator wherein the counter may be an up-counter, a down-counter or an up-down counter. For example, Ku et al [US 6,424,925 B1] show how, in an accumulator (37A) , either an up-counter or a down-counter can easily be implemented as an up-down (i.e. two-way) counter [Ku et al; Fig. 5A; col. 8, lines 8-42; col. 8, lines 8-42; col. 7, line 44 to col. 8, line 7].

(ii) Applicant's argument—"The Examiner's reliance on the claims as disclosure (reference to col. 20) is improper; In re Benno, 226 USPQ 683, 686 (Fed. Cir. 1985)" on page 3.

Examiner's response--- Examiner respectfully disagrees. Since claims 1-5 are rejected under **35 U.S.C. 102(b)** as being anticipated by Viot et al [US 5,325,341], and the published date of the Viot et al patent including **the claims** is Jun. 28, 1994; the rejection is proper. For the rejection made under **35 U.S.C. 102(b)** , any reference to In re Benno, 226 USPQ 683, 686 (Fed. Cir. 1985) is inappropriate.

(iii) Applicant's argument—"There is no disclosure of a boundary. There is no disclosure of setting to a predetermined count when the boundary is exceeded. Claims 2-5 recite additional details not disclosed in the Viot et al patent. There is no anticipation" on page 3.

Examiner's response---Examiner respectfully disagrees. Accumulator (20) is also writable, or presettable, by the CPU [Fig. 9] [Viot et al; col. 11, lines 42-45]. For

other details, Applicant is directed to the rejection of claims 2-5, as set forth in the Office action.

(iv) Applicant's argument---"Claims 6-8 were rejected as unpatentable over Viot et al when combined with additional prior art. The additional prior art overcomes none of the inadequacies in the Viot et al patent described below. There is no basis for the combination and it is not clear that the alleged combination would be operative" on page 3.

Examiner's response---- Examiner respectfully disagrees. In response to applicant's argument that there is no basis to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the additional prior art overcomes the limitations of claims 6-8 and provides motivation to combine these references, as shown in the rejection of these claims set forth in the Office action.

(v) Applicant's argument---"Claims 9-11 were rejected as unpatentable over Viot et al in view of Fu et al. There is no basis for combination" on page 3.

Examiner's response---Examiner respectfully disagrees. In response to applicant's argument that Fu et al is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Fu et al is analogous art. Therefore, the combination is appropriate.

(vi) Applicant's argument-----" Accumulator 20 is not an up-down counter. Accumulator counts to capacity and stops until reset" on page 4.

Examiner's response-----Examiner respectfully disagrees. Applicant is directed to Fig. 6 for details which shows a structure of a multi-bit pulse accumulator (20) [Fig. 6; col. 3, line 66 to col. 4, line 48; col. 4, lines 33-48; col. 11, lines 21-45]. Further, the Examiner asserts that a counter is inherent in an accumulator wherein the counter may be an up-counter, a down-counter or an up-down counter. For example, Ku et al [US 6,424,925 B1] show how, in an accumulator (37A) , either an up-counter or a down-counter can easily be implemented as an up-down (i.e. two-way) counter [Ku et al; Fig. 5A; col. 8, lines 8-42; col. 8, lines 8-42; col. 7, line 44 to col. 8, line 7].

(vii) Applicant's argument—Claim 12 was rejected as an un patentable over Viot et al in view of Ku et al, and Sharpe-Geisler. There is no basis for combination.

Examiner's response---Examiner respectfully disagrees. In response to

applicant's argument that the Sharpe-Geisler patent is nonanalogous art, it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, Sharpe-Geisler is analogous art.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Viot et al [US 5,325,341].

Regarding claim 1, Viot et al teach an accumulator (20) , as shown in Figs. 1, 6, comprising a counter [col. 3, line 66 to col. 4, line 14] and logic for preventing roll-over (logic is not shown, because it is well-known), the improvement comprising:

a first boundary for roll-over, wherein said boundary is less than the capacity of the up-down counter [Fig. 2; col. 6, lines 11-62]; and

a first multiplexer (232) coupled to the logic for preventing roll-over (logic is not shown, because it is well-known) for supplying a first predetermined count to the up-down

counter when the count in the counter is incremented past the first boundary [Figs. 1-6, 11; col. 17, line 58 to col. 18, line 68; col. 2, lines 12-47; col. 20, lines 15-22]. Further, the Examiner asserts that a counter is inherent in an accumulator wherein the counter may be an up-counter, a down-counter or an up-down counter. For example, Ku et al [US 6,424,925 B1] show how, in an accumulator (37A) , either an up-counter or a down-counter can easily be implemented as an up-down (i.e. two-way) counter [Ku et al; Fig. 5A; col. 8, lines 8-42; col. 8, lines 8-42; col. 7, line 44 to col. 8, line 7].

Regarding claim 2, Viot et al further teach the accumulator, wherein the accumulator includes logic for preventing roll-under (logic is not shown, because it is well-known), the improvement further comprising:

a second boundary for roll-under, wherein the boundary is greater than the minimum count of the up-down counter [col. 7, lines 28-39]; and

a second multiplexer (234) coupled to the logic for preventing roll-under (logic is not shown, because it is well-known) for supplying a second predetermined count to the up-down counter when the counter is decremented past the second boundary [Fig. 11; col. 18, lines 1-68; col. 20, lines 23-32].

Regarding claim 3, Viot et al further teach the accumulator comprising:
a first multiplexer (232) additionally performs the reset function (not a third multiplexer) coupled to the logic for providing reset data to the updown counter of the accumulator (20) [Fig. 11; col. 18, lines 3-4; col. 18, lines 27-30].

Regarding claim 4, Viot et al further teach the accumulator comprising: a first multiplexer (232) additionally performs the reset function (not a second multiplexer (234)) coupled to the logic for providing reset data to the updown counter of the accumulator 20 [Fig. 11; col. Col. 18, lines 137].

Regarding claim 5, Viot et al further teach the accumulator, wherein the up-down counter counts in a range of less than -n to +n, wherein n (=255) is the capacity of the counter in either direction [Fig. 6; col. 11, lines 21-45; col. 6, lines 11-33; col. 7, lines 28-39].

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 6-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viot et al as applied to claim 1 above, and further in view of either Burke [US 4,808,988] or Dillon et al [US 3, 652,838].

Regarding claim 6, Viot et al do not teach expressly the accumulator, wherein

the up-down counter counts up/down in increments of .DELTA., where .DELTA. is an integer. However, this is well-known in the art.

Burke et al teach an accumulator with an up-down counter shown in Fig. 4, wherein the up-down counter counts up/down in increments of .DELTA., where .DELTA. is an integer. However, this is well-known in the art [Figs. 4-8; col. 29, line 65 to col. 30, line 6; col. 11, lines 48-64; col. 18, lines 46-67; col. 29, lines 1-18].

Dillon et al teach an accumulator comprising an up-down counter and means for presetting an offset value when the contents of the accumulator drps below the preset limit minus the off set value [Figs. 17, 24; col. 8, lines 49-57; col. 12, line 74 to col. 13, line 8; col. 14, lines 34-40; col. 14, lines 57-63].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine either the teachings of Burke et al or Dillon et al with Viot et al in order to provide flexibility for making a wide range of choices available to the system user [Burke et al; col. 29, line 65 to col. 30, line 6] or to provide means for decoding the count in the storage address counter for enabling one discrete address in the memory element for each count value in the storage counter [Dillon et al; col. 1437-40].

Claims 7 and 8 are essentially similar to claim 6 and are rejected for the reasons stated above.

6. Claims 9-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viot et al [US 5,325,341] in view of Ku et al [US 6,424,925 B1].

Regarding claim 9, Viot et al teach an accumulator (20) , as shown in Figs. 1, 6; comprising a counter [col. 3, line 66 to col. 4, line 14] and logic for preventing roll-over (logic is not shown, because it is well-known), the improvement comprising:

a first multiplexer (232) coupled to the counter (30 & 50) and to a first count for supplying either the output from the counter or the first count to an output;
first logic (232) means coupled to the first multiplexer for causing the first multiplexer to supply either the output from the counter or the first count to the output depending upon the state of the logical output [Figs. 1-6, 11; col. 17, line 58 to col. 18, line 68; col. 2, lines 12-47; col. 20, lines 15-22]. Further, the Examiner asserts that a counter is inherent in an accumulator wherein the counter may be an up-counter, a down-counter or an up-down counter. For example, Ku et al [US 6,424,925 B1] show how, in an accumulator (37A) , either an up-counter or a down-counter can easily be implemented as an up-down (i.e. two-way) counter [Ku et al; Fig. 5A; col. 8, lines 8-42; col. 8, lines 8-42; col. 7, line 44 to col. 8, line 7].

Viot et al do not teach a first comparator producing a first logical output indicative of the comparison.

Ku et al teach a first comparator (18) coupled to the output for comparing the data on the output with a first threshold and producing a first logical output indicative of the comparison [Figs. 1E, 1F; col. 1, line 64 to col. 2, line 15].

At the time of the invention, it would have been obvious to a person of ordinary skill in the art to combine the teachings of Ku et al with Viot et al in order to detect the presence of a tone signal from the output of the first comparator [Ku et al; col. 2, lines 1-5].

Regarding claim 10, Viot et al further teach the accumulator, wherein the improvement further includes:

a second multiplexer(234) coupled to the counter (30 & 50) and to a second count for supplying either the output from the counter or the second count to the output;

second logic means (26) coupled to the second comparator and the second multiplexer for causing the second multiplexer to supply either the output from the counter or the second count to the output depending upon the state of the second logical output [Figs. 1-6, 11; col. 17, line 58 to col. 18, line 68; col. 2, lines 12-47; col. 20, lines 15-22].

Further, although Ku et al teach a first comparator (18) coupled to the output for comparing the data on the output with a first threshold and producing a first logical output indicative of the comparison [Figs. 1E, 1F; col. 1, line 64 to col. 2, line 15], at the time of the invention, it would have been obvious to a person of ordinary skill in the art to use a second comparator with a second threshold with Viot et al in order to detect the presence of a tone signal from the output of the second comparator [Ku et al; col. 2, lines 1-5].

Regarding claim 11, although Viot et al teach applying a first MUX (232) and a second MUX (234) [Fig. 11] only, it would have been obvious to one of ordinary skill in the art , at the time the invention was made, to use any number of multiplexers including a third multiplexer in order to accommodate additional counts subject to circuit, system and design constraints.

7. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Viot et al and Ku et al as applied to claim 10 above, and further in view of Sharpe-Geisler [US 6,359,466 B1].

Regarding claim 12, Viot et al do not teach expressly multiplexers connected in cascade to produce a hierarchy of outputs. However, cascading of multiplexers is well-known in the art.

Sharpe-Geisler teaches flexible circuitry including multiplexers 4 and 6 connected in cascade to produce a hierarchy of outputs wherein the second multiplexer (6) overrides the first multiplexer (4) [Fig. 3; col. 1, line 64 to col. 2, line 11], and wherein the flexible circuitry can be configured to provide an up/down counter and an accumulator [Figs. 1-9; col. 2, lines 31-34; Abstract].

Although Sharpe-Geisler teaches connecting two multiplexers in cascade, it would have been obvious to one of ordinary skill in the art , at the time the invention was made, to connect any number of multiplexers in cascade in order to produce a hierarchy of outputs subject to circuit, system and design constraints.

Conclusion

8. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ramnandan Singh whose telephone number is (571) 272-7529. The examiner can normally be reached on M-TH (8:00-5:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sinh Tran can be reached on (571) 272-7564. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ramnandan Singh
Examiner
Art Unit 2646

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